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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,709	KANAI ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-4,8-10,14-16 and 20-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,11-13 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/21/05, 12/23/04, 9/19/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II (claims 5-7, 11-13 and 17-19) in the reply filed on 25 January 2006 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

3. The three information disclosure statements (IDS) submitted on 19 September 2003, 23 December 2004, and 21 July 2005 were fully considered by the examiner.

Drawings

4. The drawings were received on 19 September 2003. These drawings are deemed acceptable for examination.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

As for claims 17-19, neither the computer readable medium, nor the computer product recited in these claims are disclosed in the specification.

Claim Objections

7. Claims 5-7, 11-13 and 17-19 are objected to because of the following informalities:

As for claim 5, "the case" recited in line 2 of the claim should be omitted for clarity. Examiner suggests replacing the modifiers with "wherein". Additionally, "the channel control units" recited in lines 4-5 of the claim should be changed to "channel control units". "Storing temporarily data" recited on page 62, line 2 should be changed to "storing temporary data" for clarity. "Storing mutually the data temporarily stored" recited in lines 6-7 of page 62 should be changed to "mutually storing the temporary data" for clarity. Finally, "transmitting the acknowledgment notifying that writing to the cache memory of the data to be written has been completed, to the information processor" as recited in the final limitation of this claim should be changed to "transmitting the acknowledgment to the information processor to notify the processor that data written to the cache memory has completed" for clarity. Similar changes are suggested, when appropriate, to claims 11 and 17, as they are similar in scope to claim 5.

As for claim 6, "storing temporarily data" recited on page 63, line 3 should be changed to "storing temporary data" for clarity. Similar changes are suggested, when appropriate, to claims 12 and 18, as they are similar in scope to claim 6.

As for claim 7, "the case" recited in line 2 of the claim should be omitted for clarity. Examiner suggests replacing the modifiers with "wherein". Additionally, "the channel control units" recited in lines 4-5 of the claim should be changed to "channel control units". "Storing temporarily data" recited on page 64, line 4 should be changed to "storing temporary data" for clarity. "The address" as recited on page 64, line 15 should be changed to "an address". Similar changes are suggested, when appropriate, to claims 13 and 19, as they are similar in scope to claim 7.

As for claim 12, "the channel control units" as recited on line 2 of the claim should be changed to "channel control units". Additionally, "the information processor" as recited on line 3 of the claim should be changed to "an information processor". "Storing temporarily data" recited on line 5 of the claim should be changed to "storing temporary data" for clarity. "Unit" on line 8 of the claim should be changed to "units". Similar changes are suggested, when appropriate to claim 18, as this claim is similar in scope to claim 12.

As for claim 17, in addition to the similar informalities addressed with claim 5, "the information processor" as recited on line 4 of this claim should be changed to "an information processor".

As for claims 7, 13 and 18, "the read-in command" as recited on line 6, page 70 (claim 13) should be changed to "the read-out command".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 5-7, 11-13 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5-7, 11-13 and 17-19 recite the limitation "the other channel control unit" (i.e. page 62, lines 14, 18 and 19 for claim 5. Though the exact line numbers are not presented here, the remaining claims recite this same limitation). There is insufficient antecedent basis for this limitation in the claim. More specifically, the preamble sets forth a “plurality of channel control units”. It is unclear, which of the plurality of channel control units is being referenced by “the other channel control unit”.

Claim 6 recites the limitation "the second cache memories" on page 63, lines 8. There is insufficient antecedent basis for this limitation in the claim as only one “second cache memory” is set forth in the preamble of this claim.

Claims 6-7, 12-13 and 18-19 recite the limitation "the cache memory" (i.e. page 63, line 21 of claim 6). There is insufficient antecedent basis for this limitation in the claim. More specifically, the preamble sets forth a both a first cache memory and a second cache memory. It is unclear, which of the cache memories is being referenced by “the cache memory”. Additionally, these claims recite “the second cache memory”

(i.e. page 68, line 27, page 69, line 1 and line 2 for claim 12). There is insufficient antecedent basis for this limitation in the claim as more than one second cache memory is set forth previously within the claim (i.e. page 68, line 22 for claim 12).

Claims 6-7, 12-13 and 18-19 additionally recite "a couple of second memories" (page 63, line 8 for claim 6 for example). The term "couple" renders the claims indefinite, as one of ordinary skill in the art would be unable to determine the metes and bounds of how many "a couple" of memories consist of. Examiner will take it "couple" to mean two.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 5-6, 11-12 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Dewey et al., hereinafter Dewey (US Patent 5,724,501).

As for claims 5, 11 and 17, Ninomiya teaches a channel control unit (as per claim 11, and method per claim 5, and medium per claim 17) in a storage control apparatus including a plurality of the channel control units each having an interface with an information processor; a disk control unit having an interface with a storage device for storing data; and a cache memory for storing temporarily data to be interchanged between the information processor and the storage device, the channel control unit comprising:

an internal connector unit (Fig. 7, element 426) for connecting mutually the cache memory (Fig. 7, elements 422 and 422'), the plurality of channel control units (Fig. 7, elements 401 and 401') and the disk control unit (Fig. 7, element 414), the cache memory being disposed in each of the plurality of channel control units connected to one another through a dedicated data transfer path used for storing mutually the stored data (Fig. 7, a plurality of cache units (element 420 and 420') are connected to the channel control units through an internal path on the bus, such that each control unit can access the cache on a dedicated bus line. The transfer path allows each host to connect to each of the respective control units. For example (referring to Fig. 7), host A can access control unit 401' via the host interface 400 to the memory interface 420, and then back to the other control unit via the single dump line 426);

a receiver for receiving data to be written from the information processor (Fig. 7, element 401 – the control unit contains logic to receive data transmitted from the host (not explicitly shown in Fig. 7)).

a writing portion for writing the data to be written to the cache memory (both the hosts and the control units are capable of writing data to the cache);

a transmitter for transmitting to the information processor the acknowledgement notifying that the writing to the cache memory of the data to be written has been completed (both the hosts and the control units are capable of receiving acknowledgements via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has

been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7).

Dewey additionally teaches a transmitter (the control unit is capable of transmitting, therefore it inherently contains a transmitter) which is capable of transmitting data to the other control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches a receiver (both the hosts and the control units are capable of receiving acknowledgements therefore they inherently possess receivers) to receive an acknowledgement sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7.

As for claims 6, 12 and 18, Dewey teaches a channel control unit (as per claim 12, and method per claim 6, and medium per claim 18) in a storage control apparatus including a plurality of the channel control units each having an interface with the information processor; a disk control unit having an interface with a storage device for storing data; a first cache memory for storing temporarily data to be interchanged between the information processor and the storage device, the first cache memory being disposed in each of the plurality of channel control unit connected to one another

by a dedicated data transfer path used for storing mutually the data temporarily stored; a couple of second cache memories for storing the same data mutually; and an internal connector unit for connecting mutually the plurality of channel control units, the disk control unit and the couple of second cache memories, the channel control unit comprising:

In his disclosure, Dewey teaches two channel control units (Fig. 7, elements 401 and 401') are connected via a dedicated data transfer path (Fig. 7, element 426 – depicts the portion of the transfer path that physically connects the control units). The transfer path allows each host to connect to each of the respective control units. For example (referring to Fig. 7), host A can access control unit 401' via the host interface 400 to the memory interface 420, and then back to the other control unit via the single dump line 426. Each control unit contains at least one cache (Fig. 7, elements 422 and 422'), and is connected to a host (Host A and Host B not shown in Fig. 7). Dewey further teaches:

a transmitter for transmitting to the second cache memory a read-in command for data stored in the second cache memory, an acquiring portion for acquiring the data from the second cache memory, a writing portion for writing the acquired data to the first cache memory (col. 2, line 54 through col. 3, line 8 – Dewey's system works by sending a request from one control unit to another. The request allows data to be copied from one control unit's cache to the other control unit's cache for data redundancy. By this means, one control unit can access data contained within the cache of the other control unit, and store said data in order to maintain data consistency within the caches);

Dewey further teaches a transmitter (the control unit is capable of transmitting therefore it inherently contains a transmitter) which is capable of transmitting data to the other control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches a receiver (both the hosts and the control units are capable of receiving acknowledgements therefore they inherently possess receivers) to receive an acknowledgement sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 5, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya et al., hereinafter Ninomiya (US PG Publication 2001/0056527 A1) in further view of Dewey.

As for claims 5, 11 and 17, Ninomiya teaches a channel control unit (as per claim 11, and method per claim 5, and medium per claim 17) in a storage control apparatus including a plurality of the channel control units each having an interface with an information processor; a disk control unit having an interface with a storage device for storing data; and a cache memory for storing temporarily data to be interchanged between the information processor and the storage device, the channel control unit comprising:

an internal connector unit (Fig. 1, element 4) for connecting mutually the cache memory (Fig. 1, element 3), the plurality of channel control units (Fig. 1, elements 1) and the disk control unit (Fig. 1, element 2), the cache memory being disposed in each of the plurality of channel control units connected to one another through a dedicated data transfer path used for storing mutually the stored data (Fig. 1, a plurality of cache units (Fig. 1, element 3) are connected to the host adaptors (i.e. channel control units) through unique internal paths on the bus, such that each control unit can access the cache on a dedicated bus line);

a receiver for receiving data to be written from the information processor (Fig. 2, element 1 – the host adaptor contains logic to receive data transmitted from the processor – paragraph 0041, all lines. Also, though not shown in Fig. 1 explicitly, each host adaptor is connected to a processor – paragraph 0036, all lines);

a writing portion for writing the data to be written to the cache memory (both the disk adaptor and host adaptor are capable of writing data to the cache – see paragraphs 0037 and 0038, all lines);

a transmitter for transmitting to the information processor the acknowledgement notifying that the writing to the cache memory of the data to be written has been completed (paragraph 0037, the host adaptor contains the logic (referring again to Fig. 2, element 1) which is used to transmit the report to the host device that writing to the cache is complete).

Ninomiya fails to teach transmitting to the other control unit and receiving the acknowledgment from the other control unit.

Dewey however teaches a quick recovery of write cache in a fault tolerant I/O system in which two channel control units (Fig. 7, elements 401 and 401') are connected via a dedicated data transfer path (Fig. 7, element 426 – depicts the portion of the transfer path that physically connects the control units). The transfer path allows each host to connect to each of the respective control units. For example (referring to Fig. 7), host A can access control unit 401' via the host interface 400 to the memory interface 420, and then back to the other control unit via the single dump line 426. Each control unit contains at least one cache (Fig. 7, elements 422 and 422'), and is connected to a host (Host A and Host B not shown in Fig. 7). In his disclosure Dewey teaches a transmitter (the control unit is capable of transmitting therefore it inherently contains a transmitter) which is capable of transmitting data to the other control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches a receiver (both the hosts and the control units are capable of receiving acknowledgements therefore

they inherently possess receivers) to receive an acknowledgement sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Ninomiya to further include Dewey's quick recovery system of write cache. By doing so, Ninomiya would benefit by having a system that is not only capable of mirroring data within his multiple control units for data recovery, but additionally one that exploits the benefits of an onboard mirroring technique, in which the hosts incur no additional latency due to the mirroring of data. This in effect can help optimize performance during normal host operation, and allow for the secondary links to be constructed with limited bandwidth, since the coping only occurs on failures as taught by Dewey (col. 2, lines 8-20).

11. Claims 7, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dewey in further view of La Fetra et al., hereinafter La Fetra (US Patent 5,155,828).

As for claims 7, 13 and 19, Dewey teaches a channel control unit (as per claim 13, and method per claim 7, and medium per claim 19) in a storage control apparatus including a plurality of the channel control units each having an interface with an information processor; a disk control unit having an interface with a storage device for

storing data; a first cache memory for storing temporarily data to be interchanged between the information processor and the storage device, the first cache memory being disposed in each of the plurality of channel control units connected to one another through a dedicated data transfer path used for storing mutually the data temporarily stored; a couple of second cache memories for storing the same data mutually; and an internal connector unit for connecting mutually the plurality of channel control units, the disk control unit and the couple of second cache memories, the channel control unit comprising:

a receiver for receiving from the information processor a read-out command for data for which the address is specified (the processor is capable of accessing data from the cache via the metadata which includes the disk and cache address for data stored in the disk or caches respectively – col. 4, lines 16-27);

a determining portion for determining whether the data at the specified address is stored in the first cache memory (a cache hit or miss can be determined –col. 7, lines 13-38. Again the determination can be made using the metadata, which directs the host to the appropriate address of the cache);

an acquiring portion for acquiring the data from the second cache memory, and a writing portion for writing the acquired data to the first cache memory (col. 2, line 54 through col. 3, line 8 – Dewey's system works by sending a request from one control unit to another. The request allows data to be copied from one control unit's cache to the other control unit's cache for data redundancy. By this means, one control unit can access data contained within the cache of the other control unit, and store said data in

order to maintain data consistency within the caches. Additionally, once a read request is encountered, data will be acquired from both cache memories – col. 7, lines 31-61);

Dewey further teaches a transmitter (the control unit is capable of transmitting therefore it inherently contains a transmitter) which is capable of transmitting data to the other control unit (Fig. 7, the memory interfaces (elements 420 and 420') are used to communicate data between the channel control units via the single dump link (data transfer path) – see also col. 2, line 54 through col. 3, line 8). Additionally, Dewey teaches a receiver (both the hosts and the control units are capable of receiving acknowledgements therefore they inherently possess receivers) to receive an acknowledgement sent via the data transfer path notifying that the writing to the cache in the other control unit is complete - col. 6, lines 45-59 – an acknowledgement can be sent since the data is stored redundantly, thus alerting the system that the data has been written. This redundancy is available to recovery data from the first control unit's cache in the case when a failure occurs in the second control unit as shown in Fig. 7. Dewey additionally teaches a transmitter for transmitting the data to the information processor (the control unit is capable of transmitting data to the host via the host interface (Fig. 7, element 400)).

Dewey fails to teach transmitting the read-out command for the data to the second cache memory if the data at the specified address is not stored in the first cache memory (rather he teaches acquiring the data from the disks – col. 7, lines 62-66).

La Fetra however teaches a computing system with a cache memory and an additional look-aside cache memory wherein a processor attempts to access a second

cache memory, and in case of a miss, accesses a first cache memory before accessing the main memory col. 2, lines 11-36). It is worthy to note that since the L2 (i.e. first cache) cache contains all of the data of L1 (i.e. second cache), Dewey would be able to maintain mirroring of the first cache by storing the same data in a section of the L2 cache in the second control unit (plus the additional data not stored in the L1 cache). This way if a miss occurs to L1, the processor can search L2 cache prior to accessing the disk.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Dewey to further include La Fetra's system with a cache memory and look-aside cache memory into his own system of mirroring data. By doing so, Dewey would have an extra level of hierarchy in his cache system in order to retrieve requested data from one of the caches, before attempting to access main memory (i.e. the disks), thereby decreasing the access time of requested memory by accessing the main memory less frequently as taught by La Fetra in col. 1, lines 25-35.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Satoh et al. (US Patent 5,568,628) teach a storage control method and apparatus for a highly reliable storage controller with multiple cache memories.

Beardsley et al. (US Patent 6,513,097 B1) teach a system for maintaining information about modified data in cache in a storage system for use during a system failure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Mano Padmanabhan 3/14/06
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER